include a first III-N material layer, a second III-N material layer, and a 2DEG channel induced in the first III-N material layer adjacent to the second III-N material layer as a result of a compositional difference between the first III-N material layer and the second III-N material layer. The first III-N material layer can include GaN. The second III-N material layer can include AlGaN or AlInGaN. A third III-N material layer can be included between the first III-N material layer and the second III-N material layer. The third III-N material layer can include AlN. The first III-N material layer and the second III-N material layer can be group III-face or [0 0 0 1] oriented or group-III terminated semipolar layers, and the second III-N material layer can be between the first III-N material layer and the electrode-defining layer. The first III-N material layer and the second III-N material layer can be N-face or [0 0 0 1 bar] oriented or nitrogen-terminated semipolar layers, and the first III-N material layer can be between the second III-N material layer and the electrode-defining layer.

[0011] The recess can extend through the entire thickness of the electrode-defining layer, or into the III-N material structure, or through the 2DEG channel. The recess can extend at least 30 nanometers into the III-N material structure. The recess can extend partially through the thickness of the electrode-defining layer. The electrode-defining layer can have a composition that is substantially uniform throughout. The electrode-defining layer can include SiN_x. A thickness of the electrode-defining layer can be between about 0.1 microns and 5 microns.

[0012] A dielectric passivation layer can be included between the III-N material structure and the electrode-defining layer, the dielectric passivation layer directly contacting a surface of the III-N material adjacent to the electrode. The dielectric passivation layer can include SiN_x. The dielectric passivation layer can be between the electrode and the III-N material structure, such that the electrode does not directly contact the III-N material structure. An additional insulating layer can be included between the dielectric passivation layer and the electrode-defining layer. The additional insulating layer can include AlN. The additional insulating layer can be less than about 20 nanometers thick.

[0013] The extending portion of the electrode can function as a field plate. The electrode can be an anode, and the device can be a diode. The electrode can be a gate, and the device can be a transistor. The device can be an enhancement-mode device, or a depletion-mode device, or a high-voltage device. The effective angle can be about 20 degrees or less, and a breakdown voltage of the device can be about 100V or larger. The effective angle can be about 10 degrees or less, and a breakdown voltage of the device can be about 300V or larger.

[0014] At least one of the steps can have a first surface that is substantially parallel to the surface of the III-N material structure and a second surface that is substantially perpendicular to the surface of the III-N material structure. At least one of the steps can have a first surface that is substantially parallel to the surface of the III-N material structure and a second surface that is slanted, the second surface forming an angle of between 5 and 85 degrees with the surface of the III-N material structure. The extending portion can directly contact the sidewall.

[0015] In another aspect, a method of forming a III-N device is described that includes forming an electrode-defining layer having a thickness on a surface of a III-N material structure, and patterning a masking layer over the electrode-defining layer, the masking layer including an opening having a width. The method also includes etching the electrode-defining layer to form a recess therein, the recess having a sidewall which comprises a plurality of steps. A portion of the recess distal from the III-N material structure has a first width, and a portion of the recess proximal to the III-N material structure has a second width, the first width being larger than the second width. The method further includes removing the masking layer, and forming an electrode in the recess, the electrode including an extending portion over the sidewall. A portion of the electrode-defining layer is between the extending portion and the III-N material structure. The etching step includes a first procedure and a second procedure, the first procedure comprising removing a portion of the electrode-defining layer, and the second procedure comprising removing a portion of the masking layer without entirely removing the masking layer. The second procedure causes an increase in the width of the opening in the masking layer.

[0016] Methods described herein can include one or more of the following. The first procedure can be performed a second time after the second procedure has been performed. The second procedure can be performed a second time after the first procedure has been performed a second time. The masking layer can include photoresist, and the photoresist in the masking layer can be redistributed prior to performing the etching step. Redistributing the photoresist can include thermally annealing the photoresist. Redistributing the photoresist can cause the masking layer to have slanted sidewalls adjacent to the opening. The etching step can result in the recess extending through the entire thickness of the electrode-defining layer. The etching step can be a first etching step, and the method can further comprise a second etching step resulting in the recess further extending into the III-N material structure.

[0017] The device can further comprise an additional dielectric layer having a thickness between the electrode-defining layer and the III-N material structure. The etching step can result in the recess further extending through the entire thickness of the additional dielectric layer. The electrode can be an anode, and the III-N device can be a diode. The electrode can be a gate, and the III-N device can be a transistor. The etching step can result in the sidewall forming an effective angle of about 40 degrees or less relative to the surface of the III-N material structure. The etching step can result in at least one of the steps in the sidewall having a first surface that is substantially parallel to the surface of the III-N material structure and a second surface that is slanted, the second surface forming an angle of between 5 and 85 degrees with the surface of the III-N material structure.

[0018] III-N devices which can be fabricated reproducibly, can support high voltages with low leakage, and at the same time can exhibit low on-resistance and high breakdown voltage, are described. Methods of forming the devices are also described. The III-N devices described herein can be transistors or diodes, and can be high-voltage devices suitable for high voltage applications. The details of one or more implementations of the invention are set forth in the accompanying drawings and description below. Other features and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0019] FIG. **1** is a cross-sectional view of a III-N HEMT device of the prior art.